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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/779,563	02/16/2004	Yoshiro Iwasa	9319S-000666	9016

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EXAMINER	
WILLIAMS, ALEXANDER O	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 03/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/779,563	IWASA, YOSHIRO	
	Examiner	Art Unit	
	Alexander O. Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2same file 2/16/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Serial Number: 10/779563 Attorney's Docket #: 9319S-00666
Filing Date: 2/16/2004; claimed foreign priority to 2/21/2003

Applicant: Iwasa

Examiner: Alexander Williams

Applicant's Amendment filed 12/19/05 to the election of the species of figures 1-9 (claims 1 to 18) filed 7/29/05, has been acknowledged. However, there are only claims 1-6 exists.

Claims 4-6 have been cancelled.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 1 to 3 are rejected under 35 U.S.C. § 102(e) as being anticipated by Lee et al. (U.S. Patent # 6,876,068 B1).

1. Lee et al. (figures 1 to 17) specifically figures 3, 4A and 4B show a lead frame for packaging **300,400** a semiconductor chip, the lead frame comprising:
a frame-shaped land **310**;
a die pad **330;**
a semiconductor chip **460** mounted to the die pad;
first to fourth support portions **320** formed in four corners of the land and supporting the die pad so that the die pad is located inside the land; and
first to fourth groups of lead members **450** having first ends and second ends that are opposite to the first ends, the first ends being fixed to the land, and the second ends being parallel in each group and connected to the semiconductor chip with a wire **480**;

wherein the lead frame can accommodate semiconductor chips **460,470** of various different sizes.

2. A lead frame according to Claim 1, Lee et al. show wherein the first to fourth groups of lead members are formed in first to fourth trapezoidal areas, the shorter bases of which face a center of the land and the longer bases of which face sides of the land, and the second ends of the first to fourth groups of lead members are along the shorter bases of the first to fourth trapezoidal areas.

3. Lee et al. (figures 1 to 17) specifically figures 3, 4A and 4B show a method for manufacturing a semiconductor device including a lead frame **300,400** having a frame-shaped land **310**; a die pad **330;** a semiconductor chip **460** mounted to the die pad; first to fourth support portions **3** formed in four corners of the land and supporting the die pad so that the die pad is located inside the land; and first to fourth groups of lead members **450** having first ends and second ends that are opposite to the first ends, the first ends being fixed to the land, and the second ends being parallel in each group and connected to the semiconductor chip with a wire, the method comprising the steps of:

cutting the first to fourth groups of lead members according to the size of the semiconductor chip to be packaged;

mounting the semiconductor chip on the die pad;

bonding the first to fourth groups of lead members and the semiconductor chip with a plurality of wires **480**;

fitting terminals to the land, for connecting the first to fourth groups of lead members to an external circuit; and

encapsulating **490** the lead frame and the semiconductor chip, wherein the lead frame can accommodate semiconductor chips **460,470** of various different sizes.

Claims 1 to 3 are rejected under 35 U.S.C. § 102(e) as being anticipated by Komatsu Kozo (Japan Patent # 4-294571).

1. Koz (figures 1 to 2) specifically figures 1a and 1b show a lead frame for packaging a semiconductor chip, the lead frame comprising:

a frame-shaped land **5**;

a die pad **2;**

a semiconductor chip **6** mounted to the die pad;

first to fourth support portions **(connected to 5 to 2)** formed in four corners of the land and supporting the die pad so that the die pad is located inside the land; and

first to fourth groups of lead members **4** having first ends and second ends that are opposite to the first ends, the first ends being fixed to the land, and the second ends **1** being parallel in each group and connected to the semiconductor chip with a wire **7**; wherein the lead frame can accommodate semiconductor chips of various different sizes.

2. A lead frame according to Claim 1, Koz show wherein the first to fourth groups of lead members are formed in first to fourth trapezoidal areas, the shorter bases of which face a center of the land and the longer bases of which face sides of the land, and the second ends of the first to fourth groups of lead members are along the shorter bases of the first to fourth trapezoidal areas.

3. Koz (figures 1 to 2) specifically figures 1a and 1b show a method for manufacturing a semiconductor device including a lead frame having a frame-shaped land **5**; a die pad **2;** a semiconductor chip **6** mounted to the die pad; first to fourth support portions **(connected to 5 to 2)** formed in four corners of the land and supporting the die pad so that the die pad is located inside the land; and first to fourth groups of lead members **4** having first ends and second ends that are opposite to the first ends, the first ends being fixed to the land, and the second ends being parallel in each group and connected to the semiconductor chip with a wire, the method comprising the steps of: cutting the first to fourth groups of lead members according to the size of the semiconductor chip to be packaged; mounting the semiconductor chip on the die pad; bonding the first to fourth groups of lead members and the semiconductor chip with a plurality of wires **7**;fitting terminals to the land, for connecting the first to fourth groups of lead members to an external circuit; and encapsulating **12** the lead frame and the semiconductor chip, wherein the lead frame can accommodate semiconductor chips of various different sizes.

Response

Applicant's arguments filed 12/19/05 have been fully considered, but are moot in view of the new grounds of rejections detailed above.

The insertion of Applicant's additional claimed language, for example, "in claim 1" cause for further search and consideration to make this action final.

Applicant's amendment necessitated the new grounds of rejection. Accordingly, **THIS ACTION IS MADE FINAL**. See M.P.E.P. ∋ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 C.F.R. ∋ 1.136(a).

A SHORTENED STATUTORY PERIOD FOR RESPONSE TO THIS FINAL ACTION IS SET TO EXPIRE THREE MONTHS FROM THE DATE OF THIS ACTION. IN THE EVENT A FIRST RESPONSE IS FILED WITHIN TWO MONTHS OF THE MAILING DATE OF THIS FINAL ACTION AND THE ADVISORY ACTION IS NOT MAILED UNTIL AFTER THE END OF THE THREE-MONTH SHORTENED STATUTORY PERIOD, THEN THE SHORTENED STATUTORY PERIOD WILL EXPIRE ON THE DATE THE ADVISORY ACTION IS MAILED, AND ANY EXTENSION FEE PURSUANT TO 37 C.F.R. ∋ 1.136(a) WILL BE CALCULATED FROM THE MAILING DATE OF THE ADVISORY ACTION. IN NO EVENT WILL THE STATUTORY PERIOD FOR RESPONSE EXPIRE LATER THAN SIX MONTHS FROM THE DATE OF THIS FINAL ACTION.

The listed references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/666,670,669,671,672,676,696,668	9/19/05 3/18/06
Other Documentation: foreign patents and literature in 257/666,670,669,671,672,676,696,668	9/19/05 3/18/06
Electronic data base(s): U.S. Patents EAST	9/19/05 3/18/06

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O. Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30AM-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alexander O Williams
Primary Examiner
Art Unit 2826

AOW
3/19/06